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materials are preferably deposited by coating or an equivalent process; their
thickness is then adjusted, for example by polishing or grinding to a value
lying between 0.05 mm and several mm.

coating at least that face of the substrate 1 bearing the metal leads 6 with a
heat-stable material 3 of the polyimide-resin or epoxy-resin kind;

This metallization step may be carried out by the sputtering or electroplating
of a metal coating containing one or more elements of the copper (Cu), nickel
(Ni), gold (Au) or similar type, with a thickness preferably lying between 5
microns and 150 microns.

In some applications, provision is made to protect the cut edge 10 of the chip
2 with a coating 11, represented only in FIG. 5, on insulating and chemically
neutral material, of the silica type or similar insulating resin, such as
preferably a polyimide capable of being deposited by photolithography (that is,
"photoimageable"), or simply by dipping into a liquid-resin bath after
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made to protect the cut edge 10 of the chip 2 with a coating 11, represented only in FIG. 5, on insulating and chemically neutral material, of the silica type or similar insulating resin, such as preferably a polyimide capable of being deposited by photolithography (that is, "photoimageable"), or simply by dipping into a liquid-resin bath after protecting at least the face bearing the metallized contacts 4.

Referring to FIG. 10, a device 30 includes a coating 31 forming a heat sink, for example a metal coating, fixed to an integrated circuit 32 forming a substrate and coated with a heat-stable and electrically insulating material 33.

Referring to FIGS. 11 and 12, a chip 35 forming a substrate is coated on the non-active face with a material 36 of the polyimide kind.

1. A semiconductor device comprising:

2. The semiconductor device accor

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reduced by the structure of the semiconductor device in which the leads 3e are
provided periodically, for example, between each pair of input and output sides
and a ground line 3E connected to a lead 3e is linked to the reinforcing plate
25 by the conductive paste film 26.

(A) First of all, a metal stacking plate 11 having a three-layer structure is
prepared as shown in FIG. 2(A). The stacking plate 11 is formed by stacking a
copper layer 12 with a typical thickness of 150 microns, an aluminum layer 13
with a typical thickness of 3 microns playing the role of an etching stopper
and a coated underlayer 14 made of copper or nickel with a typical thickness of
2 microns. It should be noted that the coated underlayer 14 can be formed into
a multi-layer structure by typically forming a nickel layer with a typical
thickness of 2 microns on a chrome layer having a typical thickness of 0.2
microns.

(B) Next, leads 3, . . . , 3 are formed on the coated underlayer 14 as shown
in FIG. 2(B). Specifically, the surface of the underlayer 14 is coated with
resist of a negative pattern for creating a pattern of the leads 3, . . . , 3.
The surface of the underlayer 14 is then covered with a coating layer made of
copper or nickel having a typical thickness of 30 microns with the resist used
as a mask. In such a process, there is no side etching. As a result, fine
leads 3, . . . , 3 can be formed with a high degree of precision. It is
preferred that an edge of the lead 3 extend from the insulating film 2 at the
terminal side of the semiconductor device because cutting or trimming of the
leads i

as is used to attach the chip 22 to the substrate 14. Alternatively, the first voltage layer 28 can also be formed integral with the substrate 14 (FIG. 3) instead of being attached by an adhesive. The first voltage layer 28 is constructed of a conductive material, metal or metal alloy, which in the preferred embodiment is preferably a metal, such as, but not limited to copper, gold, silver, nickel, aluminum, or an alloy thereof and is approximately 25-500 microns in thickness for the ring thickness. These metals are preferred because of their superior thermal and electrical conductive properties. However, other conductive materials, metals and metal alloys known to those of ordinary skill in the art can also be used, such as Copper Invar Copper.

The second voltage layer 30 comprises a plane parallel to the first voltage layer 28 and in the preferred embodiment, provides a reference voltage level to chip 22, such as a 3.3 V or 5 V power signal commonly used by integrated circuits, such as chip 22, and is constructed of a conductive material, metal or metal alloy, which in the preferred embodiment is preferably a metal, such as, but not limited to copper, gold, silver, nickel, aluminum, or an alloy thereof and is approximately 1-25 microns in thickness. The second voltage layer 30 (power) is closely coupled to the first voltage layer 28 (ground) for providing a significant level of decoupling capacitance of at least 0.05 nF/cm.sup.2. One benefit of the increased decoupling capacitance is that it allows for more simultaneous switching of data signals on the signal layer 32 without compromising